Notice of Allowability	Application No. 10/665,148	Applicant(s) YAMASAKI ET AL.	
	Examiner Jeffrie R. Lund	Art Unit 1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the after final amendment filed 4/19/05*.

2. ☒ The allowed claim(s) is/are *9,10,22 and 23*.

3. ☒ The drawings filed on *22 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☒ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: the apparatus as claimed in claims 9, 10, 22, and 23, specifically, the first group of pins and second group of pins arranged alternately along the end face of the wafer and the first group of pins and second group of pins alternatively contact the end face of the wafer (claims 9 and 22) or during a first time the first group of pins contacts the end face and the second group of pins does not, and during a second time the second group of pins contacts the end face and the first group of pins does not (claims 10 and 23) were not found in or suggest by the art.

In regard to the prior art the Examiner notes:

a. US Patent Application 2004/0231711 to Park et al (filed May 11, 2004 with a foreign priority of May 23, 2003), and JP Patent 2001-156039 (published June 8, 2001) both teach a first and second set of pins that alternately hold the end surface of the wafer, but both of the references have priority dates after the application date (March 14, 2000 with a foreign priority of March 15, 1999) of the present invention. Thus they are not available as art.

b. US Patent 5,989,342 to Ikeda et al, JP Patent 2000-100,707, JP Patent 2000-58,428, JP Patent 11-274,042, JP Patent 10-83,948, and the like all differ from the present invention in that they only include one set of pins that rotate as a single group. No suggestion or motivation was found to suggest or motivate one of ordinary skill in the art to add a second set of pins, arrange them alternately with the first set of pins, or to alternately contact the end face of the

wafer with the first then second set.

c. JP Patent 10-135312 teaches first group of pins that rotate clockwise and second group of pins that rotate counter clockwise. These pins rotate as one unit and at a steady RPM all the pins contact the end surface of the wafer. The advantage of this invention is in the acceleration and deceleration of the spin chuck. When the chuck accelerates, because of inertia, the first set of pins will less securely hold the wafer, while the second set of pins will more securely hold the wafer. When the chuck decelerates the first set of pins will securely hold the wafer, while the second set of pins will less securely hold the pin. At all times all the pins are engaged more or less securely on the end surface of the wafer. Thus the first and second groups of pins do not alternately contact the end surface of the wafer. No suggestion was found to suggest alternately contacting the first and second set of pins.

d. JP Patent 09-232410 teaches a holder with a first and second pin similar to that of US Patent Application 2004/0231711 to Park et al, and JP Patent 2001-156039, discussed above. However, JP 09-232410 teaches that the second pin is a backup to the first pin, such that when the first pin fails the second pin engages the end surface of the wafer (see paragraphs 0025-0038 of the English translation). Thus the first and second groups of pins do not alternately contact the end surface of the wafer, instead, only a single second pin will contact the end surface of the wafer, and only then upon the failure of the first pin. It is not possible to modify the reference so that the first group and second group of pins

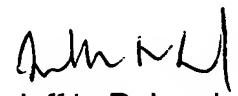
engage the end surface alternately because it would destroy the purpose of the reference (i.e. to provide a backup pin for use in the event of the failure of the first pin), Furthermore, there is no suggestion to make such a change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrie R. Lund whose telephone number is (571) 272-1437. The examiner can normally be reached on Monday-Thursday (6:30 am-6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571) 272-1435. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jeffrie R. Lund
Primary Examiner